FPGA-Based Discrete Wavelet Transforms System

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Abstract. Although FPGA technology offers the potential of designing high performance systems at low cost, its programming model is prohibitively low level. To allow a novice signal/image processing end-user to benefit from this kind of devices, the level of design abstraction needs to be raised. This approach will help the application developer to focus on signal/image processing algorithms rather than on low-level designs and implementations. This paper presents a framework for an FPGA-based Discrete Wavelet Transform system. The approach helps the end-user to generate FPGA configurations for DWT at a high level without any knowledge of the low-level design styles and architectures.

1 Introduction

The Discrete Wavelet Transform (DWT) is an efficient and useful tool for signal and image processing applications and will be adopted in many emerging standards, starting with the new compression standard JPEG2000 [1]. This growing "success" is due to the achievements reached in the field of mathematics, to its multiresolution processing capabilities, and also to the wide range of filters that can be provided. These features allow the DWT to be tailored to suit a wide range of applications [2][3].

In the early 80s, in the quest for more flexibility and rapid prototyping at low cost, custom logic based re-configurable hardware in the form of Field Programmable Gate Arrays (FPGAs) has been introduced into the IC market. However, although the fact FPGA devices offer an attractive combination of low cost, high performance, and apparent flexibility, their programming model is at the gate level. To allow an FPGA novice signal/image processing developer to benefit from the advantages offered by such devices, high level solutions are desired. It is the aim of this paper to present a framework and the preliminary results of an FPGA-based Discrete Wavelet Transforms system. The proposed environment is a Java-based Graphical User Interface (GUI) combined with both a wavelet database and a parameterised VHDL code generator.

2 The System

Initially, the architecture designer provides the library with a suite of primitive building blocks covering the various indivisible components necessary for building any new wavelet filter. The architecture designer is also responsible for updating the library with new blocks and providing the generator with efficient filter templates corresponding to a particular architecture. Due to the fact that DWT, unlike the Discrete Cosine Transform, is not unique, the filter template needs to be provided for each application with the parameters of the DWT (type, number of coefficients, 2's complement values..). The System is illustrated in Figure 1.

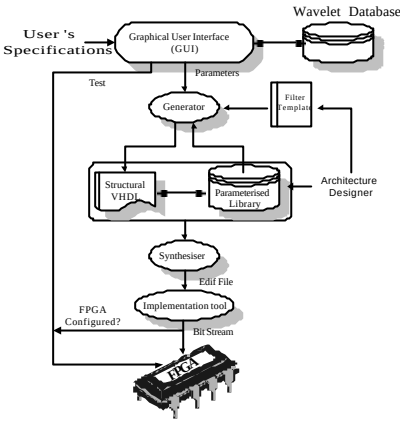

Fig.1. The FPGA-based System

For instance the user can choose between two architecture schemes: an area efficient structure and a high throughput structure. Each structure can be derived from the other either by folding or unfolding. The architectures have been derived from the architectures presented in [4][5] and partitioned adequately to ensure a maximum of hardware-macros reusability [6][7]. Even if the original architectures are VLSI-oriented (dedicated to VLSI implementations), it has been shown in [8] that efficient FPGA implementation of such regular structures can lead to good area/speed performances. Alongside, the system supports two multiplication schemes based on Baugh and Wooley algorithm. The first scheme is suitable for implementing systems with moderate throughput rate. The second one allows the implementation of high throughput rate systems through the use of a pipelined version of the first multiplication scheme. In this second case, the multiplier can be pipelined at the bit level when extended to a particular digit size [9]. More details about the multiplication and the supported wavelet structures are given in section 3 and section 4.

3 Architectures

To perform a 1-D wavelet analysis operation, a chain of processing elements combined with some delay elements, necessary for synchronisation purposes, are assembled together. The architectures used in the proposed framework for both orthonormal and biorthogonal bases are based on a time-interleaved filter's coefficient allocation approach in combination with two lines of adder [4][5]. In addition to the regularity feature, the architectures are scalable and are able to generate any wavelet filter from both families.

3.1 Architecturesfor Orthonormal DWT

Due to the fact that the high pass and low pass filters belonging to the orthonormal family are of the same length, the delay elements present a regular structure leading to a simple connection strategy between the low pass and the high pass filter [6].

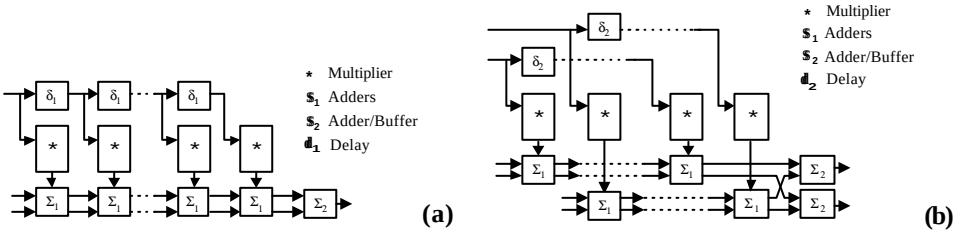

Fig.2. Generic Architecture for Orthonormal Filters
(a) Area Efficient (b) High Throughput

Figure 2 shows the generic architectures of an area efficient and a high throughput 1-D wavelet filters, respectively. The elements constituting the filters are shown on the right

hand side of each structure. The delay elements d_1 and d_2 are related by $d_1 = 2d_2$. $\sum_1$ is a combination of a demultiplexer and two bit-adders and $\sum_2$ is a combination of buffer and an bit-adder. The multiplier operators, represented by the asterisk, are similar. An orthonormal DWT is generated easily by adopting the approach proposed in [6].

3.2 Architectures for Bi-orthogonal DWT

Unlike the orthonormal basis, the high pass and the low pass filters belonging to the biorthogonal family are of different lengths. This fact leads to different connection strategies between the low pass and the high pass filters [4][7]. When designing the low level-programming model, this feature has been taken into account. Figure 3 shows the generic architectures of an area efficient and a high throughput 1-D wavelet filters, respectively. The modified delays d_{m1} and d_{m2} are combinations of d_1 , d_2 and simple adders. This choice is motivated by the fact to keep the same PE for the two supported architectures and for both bases. A biorthogonal DWT is generated easily by adopting the approach proposed in [7]. The remaining elements are similar to those involved in the orthonormal architectures.

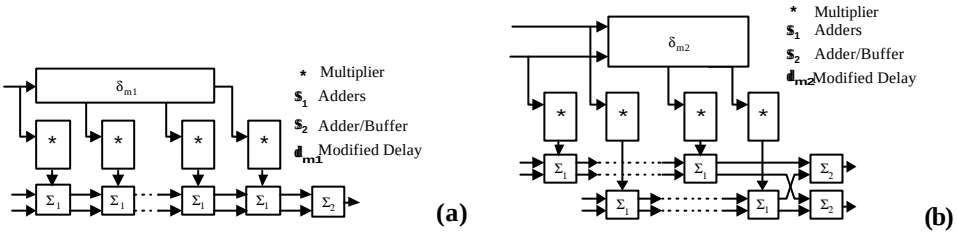

Fig.3. Generic Architecture for Biorthogonal Filters
(a) Area Efficient (b) High Throughput

4 Low Level Components

The components involved generally in any signal/image processing operation include adders, substracters, shift registers, multiplexers, demultiplexers..etc. These components are then used to generate more complicated combinations depending on the application.

4.1 Bit-level Multiplication Scheme

The most important device when building a filter-based architecture is the multiplier. To efficiently overcome the problem of handling the sign bits of the multiplier and the multiplicand of a two's complement multiplication, Baugh and Wooley algorithm is used [10]. Different structures can be envisaged to implement Baugh and wooley algorithm [10]. The structure illustrated in Figure 4 has been adopted. The structure is regular and only a single signal is used to control the required bit inversion and bit correction.

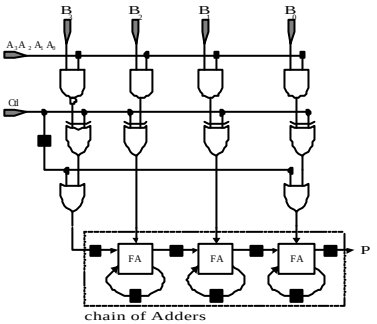

Fig.4. A Baugh and Wooley 4x4-bit 2's complement serial-paralle multiplier.

Serial-Parallel versus Digit-Parallel. In recent years, the concept of digit-serial arithmetic has been proposed as a compromise between the bit serial and the bit parallel arithmetic [11]. The systems based on this arithmetic give the DSP designers more flexibility in finding the appropriate trade-off between hardware cost and sample rate. However, due to the feedback loop associated, the multiplier obtained using traditional approach can only be pipelined at a digit level. To overcome this problem, a new algorithm that allows different level of pipelining has been developed [9]. To benefit from this approach, the chain of adders of Figure 4 needs to be adjusted to suit the algorithm [9]. In the other hand, since the filtering is based on a multiply and accumulate process, digit adders that can be pipelined at a bit level when extended to a digit size are also required. Details about pipelined digit adders can be found in [12].

4.2 Processing Element

The Processing Element (PE) is invariable through either the wavelet bases or the wavelet supported architectures. It is composed of a bit-multiplier, a demultiplexer and two 1-bit adders ($\sum_1$).

4.3 "Terminating" Element

The structure of a Terminating Element (TE) is identical for both bases and both architectures. It is composed of a bit-adder and a buffer ($\sum_2$).

4.4 Delay Elements

To handle the peculiarities of the biorthogonal and the orthonormal basis, it was decided to design two different delay modules. In the case of the orthonormal bases, the generation is easily achieved by connecting side by side either N-1 delay elements d_1 or 2(N-1) delay elements d_2. Unfortunately, the generation process in the case of the bi-orthogonal family is more complicated. More details can be found in [7].

5 Implementation Performances

To assess the effectiveness of the approach, a stage of 1-D 8 taps Daubechies wavelet pair has been generated and then implemented on the Xilinx XC4036 FPGA (speed grade-2). The XC4036 consists of 36x36 arrays of Configurable Logic Blocks (CLB) [13]. The input data and the multiplier are both 8-bits lengths. The delays d_{m1}, d_{m2}, d_1, d_2 and the buffers have been implemented efficiently by using the dedicated select-RAM distributed along each CLB. The implementation performances are resumed in Table 1.

Table 1: Implementation Performances

	Frequency	**No of CLBs**
Area Efficient (Bit Serial)	103 MHz	99
High Throughput (Bit Serial)	100 MHz	167
Area Efficient (Digit 4)	75 MHz	308
High Throughput (Digit 4)	73 MHz	615

The functionality of the bit-serial implementations has been verified using the functional and timing simulation tools of the Xilinx Foundation Software 2.1i. As it is apparent from Table 1, the FPGA area occupied by the high throughput architecture is almost double of the area efficient architecture, especially when the architecture is extended to digit size. However, the system speed remains almost unchanged for both architectures. The fact is that the critical path remains the same and the difference in speed is a consequence of routing and interconnection delays within the device.

6 Summary and Future Work

A framework for an FPGA-based Discrete Wavelet Transforms system has been presented. The methodology allows a signal/image processing application developer to generate FPGA configurations for DWT at a high level rather than spending a considerable time learning and designing at a gate and routing level. Thus, the end-user will benefit from the high performances of FPGA devices while designing at a high level with tools he is familiar with. The preliminary results are very promising; however, extensive further work needs to be done towards the extension of the system to handle different arithmetic representation, different wavelet analysis and synthesis schemes along with different architectures.

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